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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,358	01/17/2002	Chinnugounder Senthilkumar	10559/650001/P12972	5789

20985 7590 05/05/2004

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EXAMINER	
SHINGLETON, MICHAEL B	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/054,358	Applicant(s) SENTHILKUMAR ET AL.	
	Examiner Michael B. Shingleton	Art Unit 2817	

-- Th MAILING DATE f this communication appears on the cov r sh et with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/3/2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) 19-23 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18, 24-35 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

Claim Objections

Claim 31 is objected to because of the following informalities: Claim 31 is dependent upon claim 4. However, claim 4 and those claims upon which claim 4 is dependent upon do not provide proper antecedent basis for "the filtered voltage signal". Therefore, since claim 30 would provide proper antecedent basis it is assumed for examining purposes that a mere typo in the dependency of claim 31 has occurred and that the actual dependency of claim 31 is that of claim 30 and not claim 4. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 102(b) as anticipated by Clarke 6,337,604 (Clarke) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Clarke 6,337,604 (Clarke) in view of Ochiai et al. US 4,851,792 (Ochiai).

The single Figure of Clarke discloses a circuitry for controlling the oscillating frequency of an oscillator (See column 2, line 22), the circuitry having a plurality of on-chip capacitors C1-C6 (Note that the capacitors are part of the "integrated circuit" 3 and thus are on-chip capacitors.), each of which is independently selectable by a control signal D0-D5, and each of which provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22).

Claim 1 has been previously amended to recite a bias circuit to provide a substantially constant voltage to the bias at least one of the plurality of capacitors. As noted in the remarks below the examiner cannot find a reference in the original specification or disclosure to a "substantially constant voltage" as is relates to the bias voltage applied to the capacitors. Therefore, V_{bias} and V_{cc} that is considered to be a bias voltage for the capacitors in Clarke are considered to be a "substantially constant voltage". (Note that changes in V_{bias} would cause changes in the oscillator, i.e. the operating point of transistors Q1, Q3, Q4 and Q5 would change, which logically is incorrect for the typical operation of an oscillator.) However, alternatively Figure 8(a) discloses a biasing arrangement for the capacitors of an oscillator and

is configured such that the bias voltage VB of the capacitor 14 "remains constant". This as recognized by Ochiai allows for the oscillation frequency to remain constant (See column 5, around line 61).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the oscillator arrangement of Clarke with a bias arrangement that keeps the necessary bias voltage of the capacitor elements constant so as to prevent drift in oscillator frequency as taught by Ochiai.

Claims 2-6 and 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke US 6,337,604 (Clarke) in view of Ochiai et al. US 4,851,792 (Ochiai).

The same reasoning as applied to the rejection of claim 1 involving Clarke and the following: As it relates to claim 2, Clarke and Ochiai are both silent on selection of the frequency changing capacitors to be different from each other. This is merely the selection of the optimum or workable range. The values of individual capacitors is a result effective variable. This selection involves but routine skill in the art and accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the capacitance values to be any value within the optimum or workable range so as to shift the frequency in a controllable predetermined stepwise manner. One would have additionally bee motivated to do so because the selection of these result effective variables merely selects how fast the frequency is to increase or decrease. In other words given the desire to increase the frequency to follow an exponential curve the steps changes in capacitance could not be equal. They would need to be changed in value accordingly which is within the skill of one or ordinary skill in the art.

Claims 3-6 and 33 recite conventional forms of capacitors that make up the frequency changing capacitors of the oscillator. Clarke is silent on these.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted any of the conventional capacitors as recited by the claims of the instant application in place of the generic capacitors of Clarke because, as the reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitors such as the well-known capacitors as recited by the claims of the instant application.

Clarke and Ochiai are silent on the use of a filter capacitor so to generate a filtered voltage signal to bias the capacitors of the oscillator.

Figure 8a of Ochiai generically shows a constant voltage circuit and it is well known to use a filter capacitor in such circuits to as to obtain a pure a bias signal, i.e. a pure bias signal is one that contains the bias signal and no other unwanted signals like noise, AC components etc..

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a conventional constant voltage circuit that includes a filter capacitor for the constant voltage circuit of Clarke because, as the reference is silent as to the exact composition of the constant voltage circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent constant voltage circuit such as the well-known constant voltage circuit that includes a filter capacitor.

Claim 31 recites that the P-type enhancement mode MOSFET will be driven into saturation. Clarke is silent on this.

However, this involves but routine skill in the art because it is merely the selection of the optimum or workable range. The selection of biasing of a MOSFET is merely a result effective variable. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the voltage level to be such that the P-type enhancement mode MOSFET made obvious in the above combination will be operated in saturation as this is merely the selection of a result effective variable that involves but routine skill in the art.

One terminal of the capacitors is connected to a first terminal and the other terminal of the capacitors is connected to the filtered voltage is an obvious consequence of the combination made obvious above.

As noted in the previous office action, the single Figure of Clarke also discloses an electronic device comprising a real time clock, i.e. oscillator, for generating a system time signal "CLK OUT 5" (See the only Figure and column 2, around line 20.). The real time clock has a digitally tunable oscillator (Note the use of the set of shift registers 21.) for digitally adjusting an operating frequency of the real time clock to speed up or slow down the system time signal (See column 3, around line 45). Clarke also has a memory device 21 for storing data representing a configuration of the digitally adjusted tunable oscillator. Claim 35 recites the formation of a time signal that is clearly present in Clarke as noted above.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke and Ochiai as applied to claims 1-6, and 30-35 above, and further in view of Kuhn Jr. US 3,930,169 (Kuhn, Jr.).

All the same reasoning as applied in the 35 USC 102 rejection of claims 13, 16, 24, 26 and 27 and the 35 USC 103 rejection of claims 1-6, and 30-35 and the following: Clarke is silent on the composition

of the switches 9, 11, 13, 15, 17, 19(a,b) that switches the capacitors in and out of the circuit so as to change the frequency of the oscillator.

Transmission gate switches are conventional switching means as noted by Kuhn, Jr. (See Figure 1 and column 4, lines 3-29).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted conventional transmission gate switches in place of the generic switches of Clarke because, as the reference is silent as the exact switching element employed one of ordinary skill in the art would have been motivated to use any art-recognized equivalent switch such as the well-known, conventional transmission gate switch as taught by Kuhn, Jr..

As it relates to claim 8, the circuit of Clarke has a "set of registers" 21 to provide the control signals D0-D5 for selecting the individual capacitors C1-C6.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke, Ochiai and Kuhn, Jr. as applied to claims 1-8, and 30-35 above, and further in view of Horn "Basic Electronics Theory" 4th Edition pp 377-378 and pp 454-465.

As it relates to claim 9, Clarke is silent on using buffer circuitry to decouple the transmission gate switches from the set of memory registers.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

As it relates to claim 10, Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces "ripple", i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a filtered power supply to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke and Ochiai as applied to claims 1-6, and 30-35 above, and further in view of Leduc et al. US 6,400,231 (Leduc)

All the same reasoning as applied in the 35 USC 103 rejection of claims 1-6, and 30-35 the following: As it relates to claim 11, Clarke is silent on the use of an inverting amplifier as the element that provides the gain in the oscillator. Clarke utilizes the well-known differential amplifier circuit to provide gain in a crystal oscillator. However, Leduc utilizes an inverting amplifier to provide gain for the oscillator (See column 2, lines 61-62), which is an art recognized equivalent well-known way to provide gain for a crystal oscillator.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the well known differential gain arrangement of Clarke with an inverting amplifier arrangement as these are art recognized equivalent ways to provide gain to a crystal oscillator as taught by Leduc.

As it relates to claim 12, note that the single Figure of Clarke clearly shows the plurality of frequency changing capacitors as being composed of a first subset of the plurality of capacitors that is selectively electrically coupled to a first terminal of the resonator 1, and a second subset of the plurality of capacitors that is selectively electrically coupled to a second terminal of the resonator. Note that this is just giving the broadest reasonable interpretation to the claimed invention (See MPEP 904.01).

Claims 13, 15, 16 and 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horn "Basic Electronics Theory" 4th Edition pp 377-378 and pp 454-465 in view of Clarke US 6,337,604 (Clarke).

Beginning on page 420 of Horn, Horn describes the basic well-known structure of a computer. Horn describes the speed of the computer that as known by those of ordinary skill this is describing the oscillator or "real time clock" that is inherently within the computer. Also within a computer, computers inherently have a system time signal that represents at least one of hour, minute and second and this is the clock signal itself. For example 100 clock pulses will represent X number of seconds, etc.. Note that software will take this will take this and display on a monitor the hours, minutes and seconds of a day but the claims only requires a system time signal that represents at last one of hour, minute and second. Horn is silent on the specifics of the oscillator or real time clock or just clock.

The single Figure of Clarke discloses a circuitry for controlling the oscillating frequency of an oscillator (See column 2, line 22), the circuitry having a plurality of on-chip capacitors C1-C6, each of which is independently selectable by a control signal D0-D5, and each of which provides a controllable

amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22).

The single Figure of Clarke also discloses an electronic device comprising a real time clock, i.e. oscillator, for generating a system time signal "CLK OUT 5" (See the only Figure and column 2, around line 20), the real time clock having a digitally tunable oscillator (Note the use of set of shift registers 21) for digitally adjusting an operating frequency of the real time clock to speed up or slow down the system time signal (See column 3, lines 45), and a memory device 21 for storing data representing a configuration of the digitally adjusted tunable oscillator.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the conventional real time clock/oscillator circuit of Clarke for the oscillator/real time clock/clock of Horn because, as the reference is silent as the exact oscillator/clock circuit employed one of ordinary skill in the art would have been motivated to use any art-recognized equivalent switch such as the well-known, conventional oscillator/clock circuit of Clarke.

As it relates to claims like claim 15, Clarke and Ochiai are both silent on selection of the frequency changing capacitors to be different from each other. This is merely the selection of the optimum or workable range. The values of individual capacitors is a result effective variable. This selection involves but routine skill in the art and accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the capacitance values to be any value within the optimum or workable range so as to shift the frequency in a controllable predetermined stepwise manner. One would have additionally bee motivated to do so because the selection of these result effective variables merely selects how fast the frequency is to increase or decrease. In other words given the desire to increase the frequency to follow an exponential curve the steps changes in capacitance could not be equal. They would need to be changed in value accordingly which is within the skill of one or ordinary skill in the art.

Claims like claims 28 and 29 recites the frequency of oscillation as being equal to 32.768 KHz. This involves but routine skill in the art because it is merely the selection of the optimum or workable range. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the frequency to be 32,768 KHz as this involves but routine skill in the art. Additionally, one of ordinary skill in the art would have been motivated to provide any workable frequency as this is mere a selection of the result effective variable which determines how fast the microprocessor will operate.

Claims 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horn "Basic Electronics Theory" 4th Edition pp 377-378 and pp 454-465 in view of Clarke US 6,337,604 (Clarke) as applied to claims 13, 15, 16 and 24-29 above, and further in view of Theus et al. US 5,805,029 (Theus).

All the same reasoning as applied in the 35 USC 102 rejection of claims 13, 15, 16, 24, 28 and 29 following: Clarke describes in generic terms element 7 as comparing the system time signal CLK OUT 5 to be within a certain frequency range. Clarke, however, is silent on the specifics of such a structure. Note that Clarke saves the data representing the setting of the control signals in memory device 21.

Figure 4 of Theus discloses specific conventional means to compare the system time signal to the reference time signal so that a control signal can be generated to the controller of an oscillator circuit that utilizes the switching of capacitors to change the oscillator frequency. Specifically, Theus discloses receiving a reference time signal 8a and comparing this reference time signal to the system time signal 2a via a comparator 7. This controls which subsets of capacitors C11, C21, C1n, C2n that are connected to the oscillator. Note that the reference time signal just like the system time signal of Clarke represents at last one of hour, minute and second for X number of clock pulses would represent some number (including fractions) of hour(s), minute(s) and second(s).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the conventional means of Theus to compare the reference time signal to a system time signal so as to control generate the control signal because, as the Clarke reference is silent on the specific structure of the comparison arrangement 7 one of ordinary skill in the art would have been motivated to use any art-recognized equivalent frequency control means would have been usable such as the well-known conventional arrangement of Theus.

As to a communication port for the reference time signal, there is clearly a node and given the broadest reasonable interpretation of the claims consistent with the specification this node of Theus is seen as meeting this limitation. However, alternately it is well known in the art to provide separate ports so as that an external oscillator can be connected. This is what is sometimes called a calibrating source.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a separate port for the reference time signal in the combination made obvious above. One would have been motivated to do so, so that an accurate calibration signal, i.e. reference time signal can be used to accurately adjust the oscillator.

Applicant's arguments filed 6-25-2003 have been fully considered but they are not persuasive.

Applicant believes that Clarke regarding claim 1 does not disclose or suggest any bias current to bias a capacitor. The examiner respectfully disagrees. First of all the claim does not state that a bias current is to bias the capacitor(s). Claim 1 recites "a bias circuit to provide a substantially constant voltage to bias at least one of the plurality of (the) capacitors". Claim 1 recites a bias voltage not a bias current. Note that a bias voltage "Vbias" is applied to capacitors as clearly illustrated by the one and only Figure of Clarke. Also note that V_{cc} also can be considered to be a bias voltage. The examiner can't see where in the specification it mentions "substantially constant voltage" and thus the V_{bias} and the V_{cc} voltages of Clarke are seen as being substantially constant. Applicant just has not defined this term in the original disclosure. Accordingly applicant has not given a deviation like for example plus or minus ten percent is being considered substantially constant. Thus any reasonable constant bias voltage is seen as meeting this limitation. In regards to claim 1, applicant is also of the belief that "there is no suggestion that the capacitors need any bias voltage to operate". The examiner does not see a limitation in claim 1 requiring the capacitors to "need any bias voltage to operate". Applicant believes that there is "no incentive to use the floating gate MOS variable capacitor of Ochiai in the oscillator circuit of Clarke, and therefore, there is no motivation to use the bias circuit of Ochiai in the oscillator circuit of Clarke". The examiner respectfully disagrees. First of all the rejection involving claim 1 and Ochiai uses the teaching of keeping the bias voltage constant to the capacitors in an oscillator arrangement. This prevents drift in the oscillation frequency as most capacitor elements are dependent upon changes in the bias voltage applied thereto. Furthermore, the examiner respectfully disagrees with applicant that there is no motivation to have substituted various conventional capacitors for the capacitors of Clarke because, as the reference is silent as the exact construction of these capacitors one of ordinary skill in the art would have been motivated to use any art recognized equivalent capacitor as the ones as taught by Ochiai. Ochiai clearly teaches MOS capacitors connected to the ends of the crystal to set the frequency of the oscillator. This works substantially the same as Clarke. Clarke varies the overall capacitance by the selection of the capacitors switched in and out of the circuit. Just because Clarke switches capacitors in an out of the circuit does not mean that one of ordinary skill would not have found it unobvious to utilize variable capacitor elements for the capacitive elements. In fact it has been long held that making something adjustable does not present "the provision of adjustability where needed, is not a patentable advance" (See In re Stevens, 101 USPQ 284 (CCPA 1954)). One of ordinary skill in the art would have been motivated to utilize variable capacitors for the capacitors of Clarke just for the very reason of providing adjustability i.e. the individual capacitors of Clarke thereby could be calibrated, tuned, adjusted so that the change in capacitance would be accurate.

Applicant states that "it is not true that all conventional capacitors are suitable for use in oscillator circuit." and "for example, a drain-source connected P-type MOSFET may not operate properly if the biasing circuit shown in FIG. 2 (including R_{bias} and C_{bias}) were not used.". The examiner respectfully disagrees. Note above that fact that because Clarke is silent on the specific construction of the capacitor one of ordinary skill in the art would have been motivated to use any art recognized equivalent capacitor. Furthermore, it is well within the level of routine skill to provide any necessary circuitry etc. that is needed to utilize various art recognized equivalent capacitors. The issue is one of obviousness to one of ordinary skill in art and not the common engineering details that are well known to make a device work. For example just because an amplifier does not show the biasing it is well within the level of ordinary skill to provide biasing so that the device will work. The "criteria for configuring MOSFET capacitors" clearly lies within the skill of one of routine skill in the art. Note the cited references Friedman et al. 6,292,065 (Figure 3) and Kertis et al. 6,650,194.

Applicant states, "It was the applicant who first conceived of the idea of using drain-source connected MOSFETs in an oscillating circuit." Applicant is not clear when this occurred and if such was published more than one year prior to the present invention thereof by applicant. It is assumed that applicant is talking about the present invention. Thus, in response to applicant's arguments, the examiner has cited Friedman et al. 6,292,065 and Kertis et al. 6,650,194 that both have priority dates back in 2000 as showing the use of drain-source connected MOSFETs in an oscillating circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770. The examiner can normally be reached on Mon-Thurs from 8:30 to 4:30. The examiner can also be reached on alternate Fridays. The examiner normally has first Fridays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
April 1, 2004

MICHAEL B. SHINGLETON
PRIMARY EXAMINER
ART UNIT 2817